"representation". Claims 4-10 inherit the rejection from their based claim.

The Examiner has objected to the language "the optical output signal is representative of a Boolean logic output," to which Applicant disagrees. Applicant directs the Examiner's attention, for example, to Tables II and III which depict the output of a Boolean logic NAND gate and a Boolean logic AND gate, respectively. Each table shows whether inputs A and B would be light (on) or dark (off) and subsequently the related output being light (on) or dark (off). For example, in Table II, row 1, if input A is light (on) and input B is light (on), the output is dark (off). Further, if input A is light (on) and input B is dark (off), the output is light (on) (see Table II, row 2), and so on. Accordingly, the output column represents the output of a NAND gate based on the inputs A and B. Similarly, with regard to Table III, the output column provides a light and dark representation of a Boolean logic AND function based upon inputs A and B. Applicant has used the word "representative" because the light and dark (on and off states) in and of themselves are not Boolean logic outputs. Rather, the light and dark outputs are a representation of the output of the Boolean function NAND (Table II) and AND (Table III) functions based on the inputs A and B. "If the claims, read in light of the specification, reasonably apprise those skilled in the art both of the utilization and scope of the invention, and if the language is as precise as the subject matter permits," the claims are definite. Hybritech Incorporated v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1385, 231 U.S.P.Q. 81, 94, quoting Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, 624, 225 U.S.P.Q. 634, 641 (Fed. Cir. 1985).

Accordingly, Applicant respectfully submits that the specification adequately discloses what is considered to be a representation of Boolean logic output and thus the subject matter recited in claim 1 is not indefinite.

Claim Rejections – 35 U.S.C. § 102

In section 4 of the Office Action, the Examiner rejected claims 11, 36, 43 and 46 under 35 U.S.C. § 102(b) as being anticipated by the patent issued to Utaka et al. The Examiner stated:

The reasons for the rejection are set forth in the previous Office Action dated December 3, 2001.

Claims 11 and 36 have been amended to include an interference region that causes the interference between the wavefronts of the light from the optical input signal entering the interference region. Such feature has been addressed in the previous Office Action. Utaka et al. teaches that the wavefronts of the light from the optical input signals via the optical conduits (I and II) intercept and interfere with each other at the region that two conduits meets, (please see Figure 2A).

Claim 11 has been amended to have one of the at least two optical input signals being an optical bias signal. The input optical signals via either the optical conduits I or II, or Utaka et al., may be identified as the bias optical signal. Since as indicated by the applicant the bias optical signal is a light signal and Utaka et al. teaches that the input optical signals are provided as light signal, (P_o , column 3). Also the bias optical signal as one of the input optical signals must interfere with the other input signal to make the logic gate operable, this means the bias optical signal has to be coherent to the other input optical signal. The two input optical signals pass through the two conduits (I and II) of Utaka et al. are generated as light input signals and are coherent to each other, it is therefore implicitly true that one of the signals can be identified as the bias optical signal.

With regard to independent claims 11 and 36, both claims 11 and 36 recite that at least one of the two optical input signals is "an optical bias signal." The Examiner has stated that implicitly one of the signals of Utaka et al. can be identified as the bias optical signal. To this contention, Applicant disagrees.

Utaka et al. does not disclose or teach the use of an optical bias signal as described by Applicant. Applicant has explained that an optical bias signal is a constant light input that is a light input that is always in the on state. "Rejection for anticipation or lack of novelty requires, as the first step in the inquiry, that all the elements of the claimed invention be described in a single reference (citations omitted). Further, the reference must describe the applicant's claimed invention sufficiently to have placed a person of

ordinary skill in the field of the invention in possession of it." In re Spada, 15 U.S.P.Q.2d 1655, 1657 (Fed. Cir. 1990).

Because Utaka et al. does not teach or disclose a bias light input, that is a constant light used as an input to the interference region, Applicants respectfully submit that Utaka et al. does not anticipate claims 11 or 36. Again, the Applicant wishes to direct the Examiner's attention to Tables I-IV of Utaka et al., which show that input signals P1, P2, P3, and/or P4 are not used as constant light input signals. Signals P1-P4 have the range from zero to the quantity P_1. Accordingly, a constant bias light input is not provided to the interference region in Utaka et al. as described by Applicant. Therefore, Utaka et al. has not disclosed or taught Applicant's invention recited in claims 11 and 36 sufficiently to have placed a person of ordinary skill in the field of the invention in possession of the invention.

The use of an optical bias input is integral to the claimed design as it provides an efficient means in which to implement any of the desired Boolean logic functions. This efficient structure and method were not taught or disclosed by Utaka et al. Thus, Utaka et al. does not anticipate claims 11 and 36. Further, the Examiner states that Utaka et al. teaches that the input optical signals are provided as light signal (P_0, column 3), and thus suggests that P_0 is an optical bias input signal. Applicant is confused by this citation of P_0 teaching an optical bias input signal as Applicant understands P_0 as an output light signal and further as a variable (not a bias) signal. Thus, based on the Examiner's explanation, Applicant does not understand how Utaka et al. teaches the recited optical bias input signal, among other elements.

Further, Utaka et al. discloses a solid state optical processing device that requires generation and modulation of different light sources to provide light of differing wavelengths. Applicant's disclosure is directed to an integrated optical circuit in which a bias optical signal has the same wavelengths as the input signal(s). Thus, Utaka et al. fails to teach Applicant's invention.

Accordingly, for all of the reasons above, among others, Applicant respectfully submits that independent claims 11 and 36 and their respective dependents should be allowed.

Claim Rejections – 35 U.S.C. § 103

In section 6 of the Office Action, the Examiner rejected claims 1-10, 38-42 and 44-45 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Utaka et al. The Examiner stated:

> The reasons for rejection are set forth in the previous Office Action dated December 3, 2001.
>
> Claim 1 has been amended to include an interference region that causes the interference between the wavefronts of the light from the optical input signal entering the interference region. Such feature has been addressed in the previous Office Action. Utaka et al. teaches that the wavefronts of the light from the optical input signals via the optical conduits (I and II) intercept and interfere with each other at the region that two conduits meet, (please see Figure 2A).
>
> Claim 1 has been amended to have the at least two optical input signals being an optical bias signal. The input optical signals via either the optical conduits I or II, of Utaka et al., may be identified as the bias optical signal. Since as indicated by the applicant the bias optical signal is a light signal and Utaka et al. also teaches that the input optical signals are provided as light signal, (P_0 , column 3). Also the bias optical signal as one of the input optical signals must interfere with the other input signal to make the logic gate operable, this means the bias optical signal has to be coherent to the other input optical signal. The two input optical signals pass through the two conduits (I and II) of Utaka et al. are generated as light input signals and are coherent to each other, it is therefore implicitly true that one of the signals can be identified as the bias optical signal.

With regard to independent claim 1, claim 1 recites that at least one of the optical pathways is configured to transmit "an optical bias signal." The Examiner has stated that implicitly one of the signals of Utaka et al. can be identified as the bias optical signal. To

this contention, Applicant disagrees. Utaka et al. does not disclose or teach the use of an optical bias signal as described by Applicant. Applicant has explained that an optical bias signal is a constant light input that is a light input that is always in the on state. In the Office Action dated December 3, 2001, from which the Examiner has indicated that the rejection from claim 1 is inherited, the Examiner stated that Utaka et al. fails to teach "that at least one of the optical pathway transmits a biased optical signal." The Examiner has not shown how Utaka et al. teaches a bias optical input signal. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Thus, Applicant maintains that an optical bias input is missing from the disclosure of Utaka et al.

Because Utaka et al. does not teach or disclose a bias light input, that is a constant light used as an input to the interference region, Applicants respectfully submit that Utaka et al. does not render claim 1 obvious. Again, the Applicant wishes to direct the Examiner's attention to Tables I-IV of Utaka et al., which show that input signals P1, P2, P3, and/or P4 are not constant light input signals. Signals have the range from zero to the quantity P_I. Accordingly, a constant bias light input is not provided to the interference region in Utaka et al. Therefore, Utaka et al. has not described Applicant's claimed invention of claim 1 sufficiently to have placed a person of ordinary skill in the field of the invention in possession of the invention.

The use of an optical bias input is important to the claimed design as it provides an efficient means in which to implement any of the desired Boolean logic functions. This efficient structure and method were not taught or disclosed by Utaka et al. Thus, Utaka et al. does not anticipate claim 1. Further, the Examiner states that Utaka et al. teaches that the input optical signals are provided as light signal (P_o, column 3), and thus suggests that P_o is an optical bias input signal. Applicant is confused by this citation of P_o teaching an optical bias input signal as Applicant understands P_o as an output light signal and further as a variable (not a bias) signal. Thus, based on the Examiner's explanation,

Applicant d es n t understand how Utaka et al. teaches the recited optical bias input signal, among other elements.

Accordingly, Applicant respectfully submits that independent claim 1 and its respective dependents should be allowed. Also, Applicant submits that claims 38-42, which depend from independent claim 36, are allowable, because Applicant believes that independent claim 36 is allowable.

In section 7 of the Office Action, the Examiner rejected claims 13-15 and 17-22 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Utaka et al. The Examiner stated: "[t]he reasons for rejection are set forth in the previous Office Action and in the paragraphs (for claim 11) above."

Claims 13-15 and 17-22 depend from independent claim 11, which Applicant believes is allowable. Accordingly, Applicant believes that claims 13-15 and 17-22 are also allowable.

In section 8 of the Office Action, the Examiner rejected claims 31, and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over the patent issued to Yang in view of Utaka et al.

> Yang teaches a binary data processor for providing various logical functions wherein the processor comprises a coherent light source (11) for providing light through light pipes (41) serve as the plurality of optical pathways and slits (13 and 14) serves as the optical inputs to a portion such that the light from the plurality of pathways or light pipes interfere with each other, (please see Figures 4 and 5, column 4). The interference pattern is transmitted via output light pipes (42) or fiber optic bundle (43) as the optical output light signal may represent various logic functions such as AND, OR and NOT.
>
> Claim 31 has been amended to include the feature concerning the data processor being formed of optical transmission material patterned on a substrate material. It is extremely well known in the art to form optical logic circuit on a waveguide arrangement with patterned optical waveguides or pathways

in a transmission optical material on a substrate mat rial such is demonstrated by the teachings of Utaka et al. with patterned optical layer (7) on a substrate (3). (please see Figure 2A). It would have been obvious to one skilled in the art to apply the teachings of Utaka et al. to make the data processor with optical logic functions on a waveguide arrangement for the benefit of making it suited for desired applications.

Yang further teaches that logic circuit system having multiple logic steps can be constructed from combination of basic logic functions AND, OR and NOT. In Figure 6, Yang teaches a data processor system having a cascaded series of N optical processing steps that may include various combinations of the basic logic functions. Although this reference does not teach explicitly to have NOT AND (NAND) function and to have NOT and NOT AND function however since these functions are combinations of the basic logic functions, they are therefore either implicitly included or obvious modifications to one skilled in the art.

With regard to independent claim 31, claim 31 recites "the second optical input signal being an optical bias signal." As previously explained, Utaka et al. does not disclose or teach the use of an optical bias input signal as described by Applicant. Applicant has explained that an optical bias signal is a constant light input that is a light input that is always in the on state. Yang, like Utaka et al., does not teach or disclose a second optical input being an optical bias signal. Because the optical bias signal is not taught by either Yang or Utaka et al., independent claim 31 is not obvious under the combination.

Further, even if the combination of elements recited in claim 31 could be found in the combination of Utaka et al. and Yang, neither Utaka et al. nor Yang provides any teaching or motivation to combine the two references.

The Examiner states that "[i]t would have been obvious to one skilled in the art to apply the teachings of Utaka et al. to make the data processor with optical logic functions on a waveguide arrangement for the benefit of making it suited for desired applications." "[T]he Examiner can satisfy th burden of showing bviousness of the combination 'only

by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" In re Sang Su-Lee, 277 F.3d. 1338, 1343, (Fed. Cir. 2002), quoting In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). Here, the Examiner has provided no objective teaching or knowledge in the art that would provide such objective teaching.

For the reasons provided, Applicant believes that independent claim 31 is allowable. Further, claims 33-35, which depend from independent claim 31, are also allowable.

* * * * *

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date June 19, 2002 By Alistair K. Chan

FOLEY & LARDNER
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5367
Telephone: (414) 297-5730
Facsimile: (414) 297-4900

Alistair K. Chan
Attorney for Applicant
Registration No. 44,603